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**UTILITY
PATENT APPLICATION
TRANSMITTAL**
(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. KM1-001
First Inventor or Application Identifier Keiji Jono
Title Methods of Forming an Isolation etc.
Express Mail Label No. EL465686819US

1c-862 U.S. PTO 09/31/00

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
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1. ☒ * Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)

2. ☒ Specification [Total Pages 36] 1
(preferred arrangement set forth below)
- Descriptive title of the Invention Plus title pg.
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 3] 1

4. Oath or Declaration [Total Pages 3] 1
a. ☒ Newly executed (original or copy)
b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting
inventor(s) named in the prior application,
see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program (Appendix)

6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))

8. ☐ 37 C.F.R. § 3.73(b) Statement of Power of Attorney
(when there is an assignee)

9. ☐ English Translation Document (if applicable)

10. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations

11. ☐ Preliminary Amendment

12. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

13. ☐ * Small Entity Statement filed in prior application
Statement(s) ☐ Status still proper and desired
(PTO/SB/09-12)

14. ☐ Certified Copy of Priority Document(s)
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17. CORRESPONDENCE ADDRESS

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Name Frederick M. Fliegel, Ph.D.
Wells, St. John, Roberts, Gregory & Matkin P.S.

Address _____

City _____ State _____ Zip Code _____

Country _____ Telephone _____ Fax _____

Name (Print/Type) Frederick M. Fliegel, Ph.D. Registration No. (Attorney/Agent) 36,138
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TOTAL AMOUNT OF PAYMENT (\$1,740.00)

Complete if Known

Application Number	Filed Herewith
Filing Date	Filed Herewith
First Named Inventor	Keiji Jono et al.
Examiner Name	Unknown
Group / Art Unit	Unknown
Attorney Docket No.	KM1-001

METHOD OF PAYMENT (check one)

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101 690	201 345	Utility filing fee	690
106 310	206 155	Design filing fee	
107 480	207 240	Plant filing fee	
108 690	208 345	Reissue filing fee	
114 150	214 75	Provisional filing fee	

SUBTOTAL (1) (\$690.00)

2. EXTRA CLAIM FEES

Total Claims	Extra Claims	Fee from below	Fee Paid
61	20** = 41	18	738
7	3** = 4	78	312
Multiple Dependent			

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
103 18	203 9	Claims in excess of 20
102 78	202 39	Independent claims in excess of 3
104 260	204 130	Multiple dependent claim, if not paid
109 78	209 39	** Reissue independent claims over original patent
110 18	210 9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$1,050.00)

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
105 130	205 65	Surcharge - late filing fee or oath	
127 50	227 25	Surcharge - late provisional filing fee or cover sheet	
139 130	139 130	Non-English specification	
147 2,520	147 2,520	For filing a request for reexamination	
112 920*	112 920*	Requesting publication of SIR prior to Examiner action	
113 1,840*	113 1,840*	Requesting publication of SIR after Examiner action	
115 110	215 55	Extension for reply within first month	
116 380	216 190	Extension for reply within second month	
117 870	217 435	Extension for reply within third month	
118 1,360	218 680	Extension for reply within fourth month	
128 1,850	228 925	Extension for reply within fifth month	
119 300	219 150	Notice of Appeal	
120 300	220 150	Filing a brief in support of an appeal	
121 260	221 130	Request for oral hearing	
138 1,510	138 1,510	Petition to institute a public use proceeding	
140 110	240 55	Petition to revive - unavoidable	
141 1,210	241 605	Petition to revive - unintentional	
142 1,210	242 605	Utility issue fee (or reissue)	
143 430	243 215	Design issue fee	
144 580	244 290	Plant issue fee	
122 130	122 130	Petitions to the Commissioner	
123 50	123 50	Petitions related to provisional applications	
126 240	126 240	Submission of Information Disclosure Stmt	
581 40	581 40	Recording each patent assignment per property (times number of properties)	
146 690	246 345	Filing a submission after final rejection (37 CFR § 1.129(a))	
149 690	249 345	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

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SUBMITTED BY

Name (Print/Type)	Frederick M. Fliegel Ph.D.	Registration No. (Attorney/Agent)	36,138	Telephone	509-624-4276
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Complete (if applicable)

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DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures Formed in a Semiconductor, Memory Cells and DRAMS, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and

1 belief are believed to be true; and further that these statements were
2 made with the knowledge that willful false statements and the like so
3 made are punishable by fine or imprisonment, or both, under
4 Section 1001 of Title 18 of the United States Code and that such willful
5 false statement may jeopardize the validity of the application or any
6 patent issued therefrom.

7 * * * * *

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Nishiwaki, HYOGO 677-0054 JAPAN**

EL 465686819

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

*** * * * ***

**METHODS OF FORMING AN ISOLATION
TRENCH IN A SEMICONDUCTOR, METHODS
OF FORMING AN ISOLATION TRENCH IN A
SURFACE OF A SILICON WAFER, METHODS
OF FORMING AN ISOLATION TRENCH-
ISOLATED TRANSISTOR, TRENCH-ISOLATED
TRANSISTOR, TRENCH ISOLATION
STRUCTURES FORMED IN A SEMICONDUCTOR,
MEMORY CELLS AND DRAMS**

*** * * * ***

INVENTORS

**KEIJI JONO
HIROKAZU UEDA
HIROYUKI WATANABE**

ATTORNEY'S DOCKET NO. KM1-001

1 **METHODS OF FORMING AN ISOLATION TRENCH IN A**
2 **SEMICONDUCTOR, METHODS OF FORMING AN ISOLATION**
3 **TRENCH IN A SURFACE OF A SILICON WAFER, METHODS OF**
4 **FORMING AN ISOLATION TRENCH-ISOLATED TRANSISTOR,**
5 **TRENCH-ISOLATED TRANSISTOR, TRENCH ISOLATION**
6 **STRUCTURES FORMED IN A SEMICONDUCTOR, MEMORY CELLS**
7 **AND DRAMS**

8 **TECHNICAL FIELD**

9 The present invention relates to methods of forming an isolation
10 trench in a semiconductor, methods of forming an isolation trench in a
11 surface of a silicon wafer, methods of forming an isolation trench-isolated
12 transistor, trench-isolated transistor, trench isolation structures formed in
13 a semiconductor, memory cells and DRAMs.

14 **BACKGROUND OF THE INVENTION**

15 Field-effect transistors ("FETs") are used in memory structures such
16 as dynamic random access memories ("DRAMs") for controlling access
17 to capacitors used to store charge representing information contained in
18 the memories. In DRAMs, charge leakage effects necessitate periodic
19 refreshing of the information stored in the memory. In turn, refreshing
20 of the DRAM leads to increased power consumption and delays in
21 memory operation. Accordingly, it is desirable to reduce charge leakage
22 effects in DRAMs.

23 Additionally, it is desirable to minimize the area required for
24 fabrication of the elements of memories such as DRAMs. Electrical
25 isolation of various circuit elements from each other is required. In

1 turn, electrical isolation requires some of the space used on the DRAM
2 or other integrated circuitry. Various techniques have been developed
3 to reduce the amount of area needed for electrical isolation structures.
4 One technique for providing a high degree of electrical isolation while
5 requiring relatively little space is known as shallow trench isolation.

6 One source of charge leakage in DRAMs is related to carrier
7 generation-recombination phenomena. In general, lower dopant
8 concentrations tend to reduce this source of charge leakage. However,
9 other concerns tend to determine lower bounds for dopant concentrations.

10 The FETs used as access transistors determine some of these other
11 concerns. The FETs need to be able to provide a high impedance when
12 they are turned OFF, and a low impedance connection when they are
13 turned ON. DRAMs and other memories use an addressing scheme
14 whereby a wordline that is coupled to many transistor gates is selected,
15 and at the same time a bitline or digitline that is coupled to many
16 transistor drains is also selected. A FET that is located at the
17 intersection of the selected wordline and the selected bitline is turned
18 ON, and that memory cell is accessed. At the same time, many other
19 FETs have a drain voltage due to the drains of these FETs being
20 coupled to the selected bitline. These FETs exhibit some parasitic
21 conductance as a result of the drain voltage. In some types of
22 integrated circuits, a portion of that parasitic conductance is due to
23 corner effects that are an artifact of using Trench isolation techniques

1 to isolate the FETs from one another and from other circuit elements.

2 These effects are described in "Subbreakdown Drain Leakage
3 Current in MOSFET" by J. Chen et al., IEEE El. Dev. Lett., Vol.
4 EDL-8, No. 11, Nov. 1987; "Impact Of Shallow Trench Isolation On
5 Reliability Of Buried- And Surface-Channel Sub- μ m PFET" by W. Tonti
6 and R. Bolam, IEEE Cat. No. 0-7803-2031, 1995; "Shallow Trench
7 Isolation For Advanced ULSI CMOS Technologies", M. Nandakumar et
8 al.; and "Shallow Trench Isolation Characteristics With High-Density-
9 Plasma Chemical Vapor Deposition Gap-Fill Oxide For Deep-Submicron
10 CMOS Technologies", S.-H. Lee et al., Jpn. J. Appl. Phys.,
11 Vol. 37, 1998, pp. 1222-1227, which publications are hereby incorporated
12 herein by reference for their general background teachings.

13 One method of reducing these parasitic conduction effects is to
14 round the corner where the isolation trench meets the surface of the
15 semiconductor material. This may be effected by oxidizing the surface
16 of the silicon, as is described in the above-noted publications. However,
17 this approach requires additional processing steps, which tend to result
18 in reduced yield, among other things.

19 What is needed is a way to incorporate trench isolation together
20 with FETs that does not increase processing complexity and that provides
21 compact, low-leakage transistors in DRAMs and other circuitry.
22
23

SUMMARY OF THE INVENTION

In one aspect, the present invention provides a method of forming an isolation trench in a semiconductor. The method includes forming a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle. The method also includes forming a second isolation trench portion within and extending below the first isolation trench portion. The second isolation trench portion has a second depth and includes a second sidewall. The second sidewall intersects the first sidewall at an angle with respect to the surface that is greater than the first angle. A dielectric material fills the first and second isolation trench portions.

In another aspect, the present invention includes a method of forming an isolation trench in a surface of a silicon wafer. The method includes forming a mask on the surface, where the mask includes an opening and sidewalls, and etching the silicon surface using gases including CF_4 and CHF_3 in a ratio of $\text{CF}_4/\text{CHF}_3 = 0.11$ to 0.67 to form a first isolation trench portion.

In a further aspect, the present invention includes a trench-isolated transistor. The trench-isolated transistor includes first and second isolation trenches each disposed on a respective side of a portion of silicon. The first and second isolation trenches each include a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle. The first and

1 second isolation trenches each also include a second isolation trench
2 portion within and extending below the first isolation trench portion.
3 The second isolation trench portion has a second depth and includes a
4 second sidewall intersecting the first sidewall at an angle with respect to
5 the surface that is greater than the first angle. The first and second
6 isolation trenches are filled with a dielectric material. The transistor
7 further includes a gate extending across the silicon portion from the first
8 isolation trench to the second isolation trench, and source and drain
9 regions extending between the first and second isolation trench portions
10 and across the silicon portion. The source region is adjacent one side
11 of the gate and the drain region is adjacent another side of the gate
12 that is opposed to the one side.

13 14 **BRIEF DESCRIPTION OF THE DRAWINGS**

15 Preferred embodiments of the invention are described below with
16 reference to the following accompanying drawings.

17 Fig. 1 is a simplified plan view of shallow trench isolation
18 structures and a FET, in accordance with an embodiment of the present
19 invention.

20 Fig. 2 is a simplified side view, in section, taken along section
21 lines 2-2 of Fig. 1, of the shallow trench isolation structures and FET
22 of Fig. 1, in accordance with an embodiment of the present invention.
23

Fig. 3 is a simplified side view, in section, illustrating formation of a trench isolation structure, in accordance with an embodiment of the present invention.

Fig. 4 is a simplified flow chart of a process for forming the structures of Figs. 1 and 2, in accordance with an embodiment of the present invention.

Fig. 5 is a simplified schematic diagram of a memory cell that advantageously employs the structures of Figs. 1 and 2, in accordance with an embodiment of the present invention.

Fig. 6 is a simplified block diagram of a DRAM that advantageously employs the structures of Figs. 1, 2 and 5, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the Progress of Science and useful Arts" (Article 1, Section 8).

Fig. 1 shows trench isolation structures 10 and a FET 12 formed in a semiconductor substrate 13, in accordance with but one preferred embodiment of the present invention. The FET 12 includes a gate G, which may be formed from polysilicon, a source S and a drain D. The trench isolation structures 10 each include a first isolation trench portion 14 having a first depth 16 and having first sidewalls 18 each

1 intersecting a surface 20 of the semiconductor substrate 13 at a first
2 angle θ_1 .

3 The trench isolation structures 10 also each include a second
4 isolation trench portion 24 within and extending below the first isolation
5 trench portion 14. The second isolation trench portions 24 have a
6 second depth 26 and include second sidewalls 28 each intersecting one
7 of the first sidewalls 18 at a second angle θ_2 with respect to the
8 surface 20 that is greater than the first angle θ_1 to form shoulders 30
9 at the juncture of the first sidewall 18 and the second sidewall 28.

10 In one embodiment, the shoulders 30 result in substantial reduction
11 of subthreshold current through the FET 12. In other words, when the
12 FET 12 is OFF, the amount of current that can be induced in the
13 FET 12 by applying voltage to the drain D is greatly reduced.

14 In one embodiment, the first angle θ_1 is less than about sixty
15 degrees and the second angle θ_2 is eighty degrees or more. In one
16 embodiment, the first angle θ_1 is in a range of from about five degrees
17 to about forty-five degrees. In one embodiment, the first angle θ_1 is in
18 about thirty-five degrees. In one embodiment, the first angle θ_1 is about
19 forty degrees. The concerns addressed in selecting the first angle θ_1 are
20 to select an angle θ_1 providing a shoulder that reduces electrical fields
21 in the subsequently-formed FET 12 and to also select an angle that does
22 not impede subsequent filling of the trench isolation structures 10 with
23 dielectric material such as silicon dioxide.

1 Further in the illustrated embodiments, substantially straight linear
2 segment 18 extends entirely between and to outermost surface portion 20,
3 respectively, and to segment 28. Substantially straight linear segment 28
4 extends from segment 18 to a bottom of the trench isolation
5 structure 10.

6 Alternate embodiments are, of course, contemplated whereby some
7 substantially straight linear segment occurs somewhere within each of first
8 sidewalls 18 and second sidewalls 28, without extending over the entirety
9 of the first 18 and second 28 sidewalls. In the context of this patent,
10 "substantially straight linear" means a perfectly straight segment as well
11 as a segment that has a degree of curvature associated with it. A
12 curved segment is to be considered "substantially straight linear" in the
13 context of this patent provided that it has some chord length greater
14 than or equal to 30 nanometers and has some radius of curvature of at
15 least 20 nanometers.

16 The first sidewall 18 needs to incorporate a lateral dimension wide
17 enough such that wet dips occurring during processing steps such as
18 nitride hard mask removal and those subsequent up to gate oxide growth
19 do not start to etch down the sidewall of the isolation trench
20 structure 10. That dimension is proportional to the various dielectric
21 layer thicknesses, and so can vary greatly from process to process and
22 through different technology generations. Exemplary minimum extents for
23

1 the first sidewalls 18, i.e., distance from the top surface 20 to the
2 shoulder 30, are in a range of from 50 Angstroms to 500 Angstroms.

3 Fig. 3 is a simplified side view, in section, illustrating formation
4 of a trench isolation structure, in accordance with an embodiment of the
5 present invention. In one embodiment, the trench isolation structures 10
6 are created by forming a masking layer 32 on the semiconductor
7 surface 20. In one embodiment, the masking layer 32 includes a silicon
8 dioxide layer 34 having a thickness of about 100 Angstroms and a silicon
9 nitride layer 36 having a thickness of about 1000 Angstroms. A
10 photoresist layer 38 is formed on the masking layer 32, and openings 40
11 corresponding to the trench isolation structures 10 are formed in the
12 photoresist. The openings 40 have sidewalls 42.

13 In one embodiment, a plasma etch is used to form openings in the
14 masking layer 32. The plasma etch is also used to etch the first isolation
15 trench portions 14. In one embodiment, the plasma etch is performed
16 using a mixture of fluorocarbon and fluorohydrocarbon gases, such as, by
17 way of example, CF_4 , CHF_3 , CH_2F_2 and/or C_2F_8 or the like. In one
18 embodiment, the plasma etch is performed using a mixture of CF_4 and
19 CHF_3 in a ratio ranging from 0.11 to 0.67.

20 In one embodiment, the masking layer 32 is etched, and then
21 etching is continued for a predetermined time to etch the first isolation
22 trench portion 14. In one embodiment, the etching is carried out for 30
23 seconds, where the first half of the etching process is used to broach

the masking layer 32. In one embodiment, the etching is carried out for 40 seconds. A broad variety of implementations are possible, using different etch gas compositions, pressures and etch times, as may be seen by comparing these examples to the example below. In one embodiment, etching is carried out using parameters given below in Table I in a Hitachi microwave etcher model 511A, using the photoresist 38, silicon nitride 36 and silicon dioxide 34 mask structure 32 described above.

TABLE I

EXEMPLARY SHOULDER FORMATION PROCESSING PARAMETERS

Parameter	Units	Mask etch	Overetch	Trench	De-chuck
Step time	seconds	60	22	78	1.0
Gas 1	sccm	200	200	0	150
Gas 2	sccm	160	60	0	0
Gas 3	sccm	40	140	0	0
Gas 4	sccm	0	0	100	0
Gas 5	sccm	0	0	5.7	0
Pressure	mTorr	20	20	6	7.5
Power 1	W	550	550	800	1000
Power 2	W	90	130	60	0

Notes: gas 1 corresponds to argon, gas 2 corresponds to CF_4 , gas 3 corresponds to CHF_3 , gas 4 corresponds to HBr , gas 5 corresponds to O_2 , power 1 corresponds to magnetron power and power 2 corresponds to applied RF power.

The shoulder 30 is formed by a process whereby a polymer 44 is formed on the sidewalls 42. By adjusting the composition of the etching gases, applied RF power, chamber pressure and the like, the polymer 44 is formed at a rate that encourages a particular first angle θ_1 to be formed during the etching process. By stopping the etching and polymer deposition at the end of the predetermined time interval, the first

1 depth 16 can be controlled. The second isolation trench portion 24 is
2 then etched, using a different etch gas mixture, for example, as noted
3 in Table I.

4 In another embodiment, a first etch is carried out to provide the
5 first isolation trench portion 14. A second masking step is then carried
6 out, and openings corresponding to the second isolation trench
7 portion 24 are created. The second isolation trench portion 24 is then
8 etched.

9 In one embodiment, the first depth 16 is chosen to be five to
10 thirty or fifty percent of the total trench depth, i.e., the first depth 16
11 plus the second depth 26. In one embodiment, the first depth 16 is
12 chosen to be five to fifteen percent of the total trench depth. In one
13 embodiment, bottoms of the trenches are implanted with dopant after the
14 first 14 and second 24 trench portions are etched. This allows a
15 shallower trench to be employed, and results in the first depth 16 being
16 a larger percentage of the total trench depth.

17 In one embodiment, implant doses required to form the source S
18 and drain D regions are reduced by as much as ten percent when the
19 shoulder 30 is present, resulting in an increase of as much as thirty
20 percent of the time required between refresh cycles. For example, if a
21 typical implant dose of $5.4 \times 10^{12}/\text{cm}^2$ were ordinarily required to dope
22 channel regions, a dose of $4.9 \times 10^{12}/\text{cm}^2$ could be employed together with
23 formation of the shoulder 30.

1 Following etching of the first 14 and second 24 isolation trench
2 portions, the photoresist layer 38 and the polymer 44 may be stripped
3 using a conventional oxygen ashing process. A dielectric material,
4 typically silicon dioxide, may be used to fill the first 14 and second 24
5 isolation trench portions, and conventional chemical-mechanical polishing
6 may be used to planarize the resultant structure. In one embodiment,
7 plasma etchback is employed to planarize the dielectric material, usually
8 together with another patterning step or a planarizing coating layer. The
9 gate G may be formed using conventional polysilicon, polycide or metal,
10 and the source S and drain D may be formed using conventional ion
11 implantation techniques or doping outdiffusion from subsequent layers.

12 Fig. 4 is a simplified flow chart of a process P1 for forming the
13 structures of Figs. 1 and 2, in accordance with an embodiment of the
14 present invention.

15 In a step S1, the first isolation trench portions 14 are formed.
16 In one embodiment, the first isolation trench portions 14 are formed by
17 forming the masking layer 32, followed by plasma etching, as described
18 above.

19 In a step S2, the second isolation trench portions 24 are formed.
20 In one embodiment, the second isolation trench portions 24 are formed
21 by etching as described above with reference to Fig. 3 and Table I. In
22 one embodiment, the second isolation trench portions 24 are formed by
23 separate masking and etching operations.

1 In a step S3, the first 14 and second 24 trench portions are filled
2 with a dielectric using conventional processing techniques as described
3 above. The step S3 may include planarization of the dielectric material,
4 for example via conventional chemical-mechanical polishing.

5 In a step S4, the FET 12 is formed, using conventional processing
6 techniques, as discussed above. The process P1 then ends, and
7 processing continues using conventional processing operations.

8 Fig. 5 is a simplified schematic diagram of a memory cell 50 that
9 advantageously employs the structures of Figs. 1 and 2, in accordance
10 with an embodiment of the present invention. The memory cell 50
11 includes the FET 12 of Figs. 1 and 2, a capacitor 52 coupled to the
12 source S of the FET 12, a wordline 54 coupled to the gate G (and to
13 other gates in other memory cells) and a bitline 56 coupled to the
14 drain D of the FET 12 (and to other drains in other memory cells).
15 By selecting the wordline 54 and the bitline 56, the FET 12 is turned
16 ON, and charge stored in the capacitor 52 can then be measured to
17 determine the datum stored in the memory cell 50. Alternatively, by
18 selecting and turning the FET 12 ON, charge can be injected into the
19 capacitor 52 to write a datum therein, and the FET 12 can then be
20 turned OFF to store the datum in the memory cell 50.

21 Fig. 6 is a simplified block diagram of a DRAM 60 that
22 advantageously employs the structures of Figs. 1, 2 and 5, in accordance
23 with an embodiment of the present invention. The DRAM 60 includes

1 a memory cell array 62 coupled to a group of wordlines 56 and a group
2 of bitlines 54. Address decoders, such as a row decoder 64 and a
3 column decoder 68, decode addresses provided via a bus, allowing data
4 to be read from or written to memory cells 50 in the memory cell
5 array 62.

6 In compliance with the statute, the invention has been described
7 in language more or less specific as to structural and methodical
8 features. It is to be understood, however, that the invention is not
9 limited to the specific features shown and described, since the means
10 herein disclosed comprise preferred forms of putting the invention into
11 effect. The invention is, therefore, claimed in any of its forms or
12 modifications within the proper scope of the appended claims
13 appropriately interpreted in accordance with the doctrine of equivalents.
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CLAIMS:

1. A method of forming an isolation trench in a semiconductor comprising:

forming a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

filling the first and second isolation trench portions with dielectric material.

2. The method of claim 1, wherein forming a second isolation trench portion includes forming the second angle to be between eighty and ninety degrees.

3. The method of claim 1, wherein forming a first isolation trench portion includes forming the first angle to be in a range of from about thirty degrees to about seventy degrees and forming a second isolation trench portion includes forming the second angle to be more than eighty degrees.

1 4. The method of claim 1, wherein forming an isolation trench
2 in a semiconductor comprises forming an isolation trench in silicon.

3
4 5. The method of claim 1, wherein forming a first isolation
5 trench portion comprises:

6 forming a silicon nitride layer on the semiconductor surface;

7 forming a masking layer having an opening disposed therein atop
8 the silicon nitride layer, the opening including sidewalls;

9 plasma etching through the silicon nitride layer using conditions that
10 also deposit a polymer on the sidewalls;

11 continuing etching for a predetermined time interval after the
12 silicon nitride layer has been broached and continuing to deposit polymer
13 on the sidewalls; and

14 stopping the etching and depositing at the end of the
15 predetermined time interval.

16
17 6. The method of claim 5, wherein etching and depositing
18 comprises:

19 providing a mixture of gasses chosen from a group consisting of
20 CF_4 , CHF_3 , CH_2F_2 and C_2F_8 ; and

21 supplying radio frequency excitation to the mixture.
22
23

1 7. The method of claim 5, wherein etching and depositing
2 comprises:

3 providing fluorocarbon gases; and
4 supplying radio frequency excitation to the mixture.
5

6 8. The method of claim 1, wherein forming the first isolation
7 trench portion comprises plasma etching the first isolation trench portion
8 using gases including CF_4 and CHF_3 in a ratio of $\text{CF}_4/\text{CHF}_3 = 0.11$
9 to 0.67.
10

11 9. The method of claim 1, wherein forming the first isolation
12 trench portion comprises:

13 forming a silicon nitride layer on the semiconductor surface;

14 forming a masking layer having an opening disposed therein atop
15 the silicon nitride layer, the opening including sidewalls;

16 plasma etching through the silicon nitride layer using gases including
17 CF_4 and CHF_3 in a ratio of $\text{CF}_4/\text{CHF}_3 = 0.11$ to 0.67;

18 depositing a polymer on the sidewalls during plasma etching;

19 continuing etching for a predetermined time after the silicon nitride
20 layer has been broached and continuing depositing polymer on the
21 sidewalls; and

22 stopping etching and depositing when the predetermined interval
23 ends.

1 10. The method of claim 1, wherein forming a first isolation
2 trench portion comprises forming a first isolation trench portion having
3 a first depth of between five and fifty percent of a total trench depth.
4

5 11. The method of claim 1, further comprising planarizing the
6 dielectric material filling the first and second isolation trench portions.
7

8 12. The method of claim 1, wherein forming a first isolation
9 trench portion comprises forming a first isolation trench portion including
10 a sidewall at least some of which forms a substantially straight linear
11 segment.
12

13 13. A method of forming an isolation trench in a surface of a
14 silicon wafer comprising:
15

16 forming a mask on the surface, the mask including an opening and
17 sidewalls; and
18

19 etching the silicon surface using gases including CF_4 and CHF_3 in
20 a ratio of $\text{CF}_4/\text{CHF}_3 = 0.11$ to 0.67 to form a first isolation trench
21 portion.
22
23

1 14. The method of claim 13, wherein etching the silicon surface
2 includes forming a first isolation trench portion having a first sidewall
3 that intersects the silicon surface at an angle in a range of from about
4 thirty degrees to about seventy degrees.

5
6 15. The method of claim 14, wherein forming a first isolation
7 trench portion comprises forming a first isolation trench portion including
8 a sidewall at least some of which forms a substantially straight linear
9 segment.

10
11 16. The method of claim 13, further comprising forming a second
12 isolation trench portion within and extending below the first isolation
13 trench portion, the second isolation trench portion including a second
14 sidewall intersecting the first sidewall at an angle with respect to the
15 surface that is greater than the first angle.

16
17 17. The method of claim 16, wherein forming a first isolation
18 trench portion comprises forming a first isolation trench portion having
19 a first depth of between five and fifty percent of a total trench depth.

1 18. The method of claim 17, further comprising:
2 filling the first and second isolation trench portions with dielectric
3 material; and
4 planarizing the dielectric material filling the first and second
5 isolation trench portions.
6

7 19. The method of claim 13, wherein forming a mask comprises:
8 forming a silicon nitride layer on the semiconductor surface; and
9 forming a masking layer having an opening disposed therein atop
10 the silicon nitride layer, the opening including sidewalls.
11

12 20. The method of claim 19, wherein etching the surface
13 comprises:
14

15 plasma etching through the silicon nitride layer;
16 continuing etching for a predetermined time interval after the
17 silicon nitride layer has been broached and continuing to deposit polymer
18 on the sidewalls; and
19

20 stopping the etching and depositing at the end of the
21 predetermined time interval.
22
23

1 21. The method of claim 19, further comprising forming a second
2 isolation trench portion within and extending below the first isolation
3 trench portion, the second isolation trench portion having a second depth
4 and including a second sidewall intersecting the first sidewall at an angle
5 with respect to the surface that is greater than the first angle.

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1 22. A method of forming an isolation trench-isolated transistor
2 comprising:

3 forming first and second isolation trenches disposed to a respective
4 side of a portion of silicon, forming the first and second isolation
5 trenches comprising:

6 forming a mask on the surface, the mask including first and
7 second openings corresponding to the first and second isolation
8 trenches;

9 forming a first isolation trench portion in each of the first
10 and second openings, each first isolation trench portion having a
11 first depth and having a first sidewall intersecting a surface of the
12 semiconductor at a first angle; and

13 forming a second isolation trench portion within and
14 extending below each of the first isolation trench portions, the
15 second isolation trench portions having a second depth and
16 including a second sidewall intersecting a respective one of the first
17 sidewalls at an angle with respect to the surface that is greater
18 than the first angle; the method further comprising:

19 filling the first and second isolation trench portions with dielectric
20 material;

21 forming a gate extending across the silicon portion from the first
22 isolation trench to the second isolation trench; and

23 forming source and drain regions extending between the first and

1 second isolation trench portions, the source region being disposed adjacent
2 one side of the gate and the drain region being disposed adjacent
3 another side of the gate that is opposed to the one side.

4
5 23. The method of claim 22, wherein forming a first isolation
6 trench portion comprises etching the silicon surface using gases including
7 CF_4 and CHF_3 in a ratio of $\text{CF}_4/\text{CHF}_3 = 0.11$ to 0.67 .

8
9 24. The method of claim 22, wherein forming a mask comprises:
10 forming a silicon nitride layer on the semiconductor surface; and
11 forming a masking layer having an opening disposed therein atop
12 the silicon nitride layer, the opening including sidewalls.

13
14 25. The method of claim 22, wherein forming a first isolation
15 trench portion comprises:

16 plasma etching through the silicon nitride layer using conditions that
17 also deposit a polymer on the sidewalls;

18 continuing etching for a predetermined time after the silicon nitride
19 layer has been broached and continuing to deposit polymer on the
20 sidewalls; and

21 stopping the etching and depositing at the end of the
22 predetermined interval.

1 26. The method of claim 25, wherein plasma etching comprises
2 etching using gases including CF_4 and CHF_3 in a ratio of
3 $\text{CF}_4/\text{CHF}_3 = 0.11$ to 0.67 .
4

5 27. The method of claim 22, wherein forming a first isolation
6 trench portion comprises forming a first isolation trench portion having
7 a first sidewall intersecting a surface of the semiconductor at an angle
8 in a range of from about thirty degrees to about seventy degrees.
9

10 28. The method of claim 22, wherein forming a first isolation
11 trench portion comprises forming a first isolation trench portion including
12 a sidewall at least some of which forms a substantially straight linear
13 segment.
14

15 29. The method of claim 27, wherein forming a second isolation
16 trench portion comprises forming a second isolation trench portion having
17 a second sidewall forming an angle of more than eighty degrees with the
18 surface.
19

20 30. The method of claim 22, wherein forming a first isolation
21 trench portion comprises forming a first isolation trench portion having
22 a first depth of between five and fifty percent of a total trench depth.
23

1 31. The method of claim 30, further comprising planarizing the
2 dielectric material filling the first and second isolation trench portions.

3
4 32. The method of claim 22, wherein forming a gate comprises
5 forming a gate comprising polysilicon.
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1 33. A trench-isolated transistor comprising:

2 first and second isolation trenches each disposed on a respective
3 side of a portion of silicon, the first and second isolation trenches each
4 comprising:

5 a first isolation trench portion having a first depth and
6 having a first sidewall intersecting a surface of the silicon at a first
7 angle;

8 a second isolation trench portion within and extending below
9 the first isolation trench portion, the second isolation trench portion
10 having a second depth and including a second sidewall intersecting
11 the first sidewall at an angle with respect to the surface that is
12 greater than the first angle; and

13 a dielectric material filling the first and second isolation
14 trench portions, the transistor further comprising:

15 a gate extending across the silicon portion from the first
16 isolation trench to the second isolation trench; and

17 source and drain regions extending between the first and
18 second isolation trench portions and across the silicon portion, the
19 source region being disposed adjacent one side of the gate and the
20 drain region being disposed adjacent another side of the gate that
21 is opposed to the one side.
22
23

1 34. The trench-isolated transistor of claim 33, wherein the first
2 isolation trench portion comprises a sidewall at least some of which forms
3 a substantially straight linear segment.
4

5 35. The trench-isolated transistor of claim 33, wherein the second
6 angle is between eighty and ninety degrees.
7

8 36. The trench-isolated transistor of claim 33, wherein the first
9 angle is in a range of from about thirty degrees to about seventy degrees
10 and the second angle is more than eighty degrees.
11

12 37. The trench-isolated transistor of claim 33, wherein the first
13 isolation trench portion has a first depth of between five and fifty
14 percent of a total trench depth.
15

16 38. The trench-isolated transistor of claim 33, wherein the
17 dielectric material filling the first and second isolation trench portions has
18 a planar surface.
19

20 39. The trench-isolated transistor of claim 33, wherein the first
21 angle is in a range of from about thirty degrees to about seventy
22 degrees.
23

1 40. The trench-isolated transistor of claim 39, wherein the second
2 angle is in a range of from eighty to ninety degrees.

3
4 41. The trench-isolated transistor of claim 33, wherein the
5 transistor is formed as a part of a memory integrated circuit.

6
7 42. A trench isolation structure formed in a semiconductor
8 comprising:

9 a first isolation trench portion having a first depth and having a
10 first sidewall intersecting a surface of the semiconductor at a first angle;

11 a second isolation trench portion within and extending below the
12 first isolation trench portion, the second isolation trench portion having
13 a second depth and including a second sidewall intersecting the first
14 sidewall at an angle with respect to the surface that is greater than the
15 first angle; and

16 a dielectric material filling the first and second isolation trench
17 portions.

18
19 43. The trench isolation structure of claim 42, wherein the first
20 isolation trench portion comprises a sidewall at least some of which forms
21 a substantially straight linear segment.

1 44. The trench isolation structure of claim 42, wherein the first
2 angle is in a range of from about thirty degrees to about seventy degrees
3 and the second angle is more than eighty degrees.

4
5 45. The trench isolation structure of claim 42, wherein the first
6 angle is in a range of from about thirty degrees to about seventy
7 degrees.

8
9 46. The trench isolation structure of claim 42, wherein the first
10 isolation trench portion has a first depth of between five and fifty
11 percent of a total trench depth.

12
13 47. The trench isolation structure of claim 42, wherein the trench
14 isolation structure is formed in a memory integrated circuit.

1 48. A memory cell including:
2 a capacitor;
3 a trench-isolated transistor having a gate, a drain and a source, the
4 source being coupled to one terminal of the capacitor, the trench-isolated
5 transistor including:
6 first and second isolation trenches each disposed on a respective
7 side of a portion of silicon, the first and second isolation trenches each
8 comprising:
9 a first isolation trench portion having a first depth and
10 having a first sidewall intersecting a surface of the silicon at a first
11 angle;
12 a second isolation trench portion within and extending below
13 the first isolation trench portion, the second isolation trench portion
14 having a second depth and including a second sidewall intersecting
15 the first sidewall at an angle with respect to the surface that is
16 greater than the first angle; and
17 a dielectric material filling the first and second isolation
18 trench portions;
19 the transistor further comprising:
20 a gate extending across the silicon portion from the first
21 isolation trench to the second isolation trench; and
22 source and drain regions extending between the first and
23 second isolation trench portions and across the silicon portion, the

1 source region being disposed adjacent one side of the gate and the
2 drain region being disposed adjacent another side of the gate that
3 is opposed to the one side;

4 the memory cell further including:

5 a bitline coupled to the drain; and

6 a wordline coupled to the gate.

7
8 49. The memory cell of claim 48, wherein the gate comprises
9 polysilicon.

10
11 50. The memory cell of claim 48, wherein the first isolation
12 trench portion comprises a sidewall at least some of which forms a
13 substantially straight linear segment.

14
15 51. The memory cell of claim 48, wherein the first angle is in
16 a range of from about thirty degrees to about seventy degrees and the
17 second angle is more than eighty degrees.

18
19 52. The memory cell of claim 48, wherein the first angle is in
20 a range of from about thirty degrees to about seventy degrees.
21
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23

1 53. The memory cell of claim 48, wherein the first isolation
2 trench portion has a first depth of between five and fifty percent of a
3 total trench depth.

4
5 54. The memory cell of claim 48, wherein the memory cell is
6 included within a DRAM integrated circuit.

1 55. A DRAM comprising:
2 address decoding circuitry;
3 a group of bitlines coupled to the address decoding circuitry and
4 extending in a first direction;
5 a group of wordlines coupled to the address decoding circuitry and
6 extending in a second direction, each wordline in the group of wordlines
7 intersecting each of the bitlines in the group of bitlines once at an
8 intersection;
9 a plurality of memory cells each disposed at one of the
10 intersections, each memory cell comprising:
11 a capacitor;
12 a trench-isolated transistor having a gate, a drain and a
13 source, the source being coupled to one terminal of the capacitor,
14 the trench-isolated transistor including:
15 first and second isolation trenches each disposed on a
16 respective side of a portion of silicon, the first and second isolation
17 trenches each comprising:
18 a first isolation trench portion having a first depth and
19 having a first sidewall intersecting a surface of the silicon at
20 a first angle;
21 a second isolation trench portion within and extending
22 below the first isolation trench portion, the second isolation
23 trench portion having a second depth and including a second

1 sidewall intersecting the first sidewall at an angle with respect
2 to the surface that is greater than the first angle; and
3 a dielectric material filling the first and second isolation
4 trench portions;
5 the transistor further comprising:

6 a gate extending across the silicon portion from the
7 first isolation trench to the second isolation trench; and

8 source and drain regions extending between the first
9 and second isolation trench portions and across the silicon
10 portion, the source region being disposed adjacent one side
11 of the gate and the drain region being disposed adjacent
12 another side of the gate that is opposed to the one side;

13 each memory cell further including:

14 one bitline of the group of bitlines coupled to the drain; and
15 one wordline of the group of wordlines coupled to the gate.

16
17 56. The DRAM of claim 55, wherein the first isolation trench
18 portion comprises a sidewall at least some of which forms a substantially
19 straight linear segment.

20
21 57. The DRAM of claim 55, wherein the gate comprises
22 polysilicon.
23

1 58. The DRAM of claim 55, wherein the first angle is in a range
2 of from about thirty degrees to about seventy degrees and the second
3 angle is more than eighty degrees.

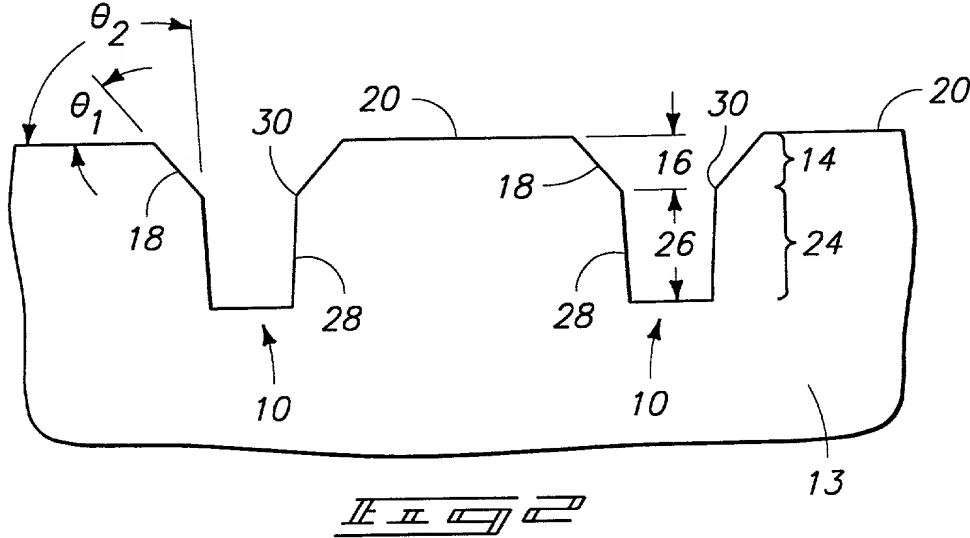
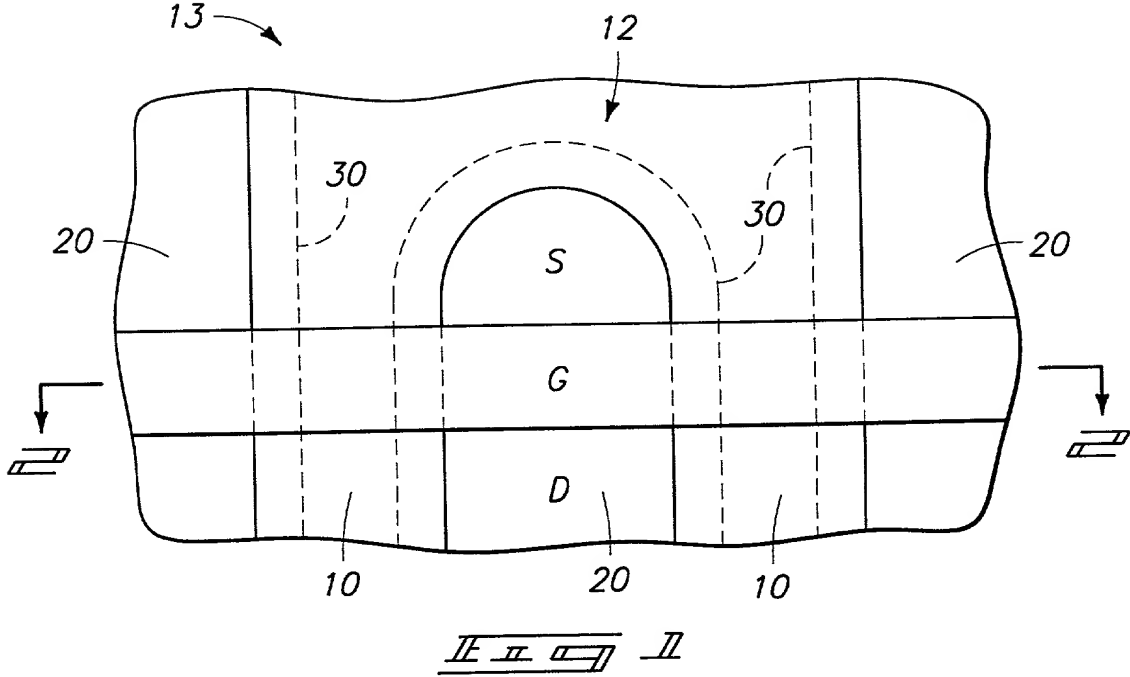
4
5 59. The DRAM of claim 55, wherein the first angle is in a range
6 of from about thirty degrees to about seventy degrees.

7
8 60. The DRAM of claim 55, wherein the first isolation trench
9 portion has a first depth of between five and fifty percent of a total
10 trench depth.

11
12 61. The DRAM of claim 55, wherein the dielectric material filling
13 the first and second isolation trench portions includes a planar outer
14 surface.

1 **ABSTRACT OF THE DISCLOSURE**

2 A method of forming an isolation trench in a semiconductor
3 includes forming a first isolation trench portion having a first depth and
4 having a first sidewall intersecting a surface of the semiconductor at a
5 first angle. The method also includes forming a second isolation trench
6 portion within and extending below the first isolation trench portion. The
7 second isolation trench portion has a second depth and includes a second
8 sidewall. The second sidewall intersects the first sidewall at an angle
9 with respect to the surface that is greater than the first angle. A
10 dielectric material fills the first and second isolation trench portions.
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